



# UNITED STATES PATENT AND TRADEMARK OFFICE

*CU*

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,142	12/17/2001	Hirotooshi Kubo	492322002600	4143
25227	7590	10/02/2003		
MORRISON & FOERSTER LLP 1650 TYSONS BOULEVARD SUITE 300 MCLEAN, VA 22102			EXAMINER LATTIN, CHRISTOPHER W	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 10/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/016,142

Applicant(s)

KUBO ET AL.

Examiner

Christopher W Lattin

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) 1-8 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 9-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakashima (5,811,871, cited by applicant).

Nakashima et al. teach a method for manufacturing a semiconductor device comprising the steps of: forming a base region 30 of a first conducting type on a surface of a collector layer 4 of a second conducting type; forming a polysilicon base electrode layer 15 on a surface of the base region and forming an insulating film 31 on a surface of the base electrode layer; forming a trench 32 (see Fig. 41), which does not reach the collector layer, in the base region by creating an opening at a part of the base electrode layer and the insulating film and forming a sidewall 35 on an inside wall of the trench, thus forming a γ-shaped trench; forming a polysilicon layer 37 containing impurities for emitter diffusion inside the trench, forming an emitter region 38 by diffusing the impurities of the polysilicon layer; and forming a through hole on the insulating film so as to form a base electrode 41 which comes into contact with the base electrode layer 15 and at the same time forming an emitter electrode 41 which comes into contact with the polysilicon layer. See Figures 4, 30-43.

Claims 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshihara (5,789,285).

Yoshihara teaches a method for manufacturing a semiconductor device comprising the steps of: preparing a collector layer 63 of a first conducting type; forming a base electrode layer 43 made of polysilicon containing impurities of a second conducting type on a surface of the collector layer and forming an insulating film 54 on the surface of the base electrode layer; forming a trench 55 in the collector layer by creating an opening at a part of the base electrode layer and the insulating film and doping impurities of the second conducting type so that a doped region 84 is formed around the trench and in the base electrode layer; forming a sidewall 56 on an inside wall of the trench; forming a polysilicon layer 86 containing impurities for emitter diffusion inside the trench; diffusing the impurities of the second conducting type of the doped region for forming a base region 94 and, at the same time, diffusing the impurities of the polysilicon layer for forming an emitter region 93, and forming a through hole on the insulating film and forming a base electrode 51 which comes into contact with the base electrode layer and, at the same time, forming an emitter electrode 51 which comes into contact with the polysilicon layer, wherein the trench is formed as a  $\gamma$ -shaped trench. See Figures 2 and 3A-3K.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher Lattin whose telephone number is (703)

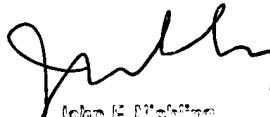
Art Unit: 2812

305-3017. The examiner can normally be reached Monday through Friday from 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached at (703) 308-3325. The fax number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

CWL   
September 24, 2003

  
John H. Niebling  
Supervisory Patent Examiner  
Technology Center 2800